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AMENDMENTS TO THE CLAIMS

Claim 1. (previously presented) Carrier recovery means - in particular in a channel decoding unit and/or a digital demodulating unit being particularly provided in a digital broadcasting receiver - for recovering a carrier of a received digital input signal, comprising at least first and second phase error detecting means, in which:

said first phase error detecting means is adapted for detecting a robust estimate for the phase error of the received digital input signal and for generating and outputting a robust phase error signal representative of said robust phase error,

said second phase error detecting means is adapted for receiving the robust phase error signal from said first phase error detecting means and for deriving therefrom a frequency sensitive phase error signal which is representative of the sign of the frequency error with respect to the received digital input signal, and

said frequency sensitive phase error signal is used to reduce the frequency error with respect to the received digital signal to enable locking to at least the carrier thereof.

Claim 2. (previously presented) Carrier recovery means according to claim 1, **characterized in** that said second phase error detecting means comprises at least a subtracting / differentiating unit, a first limiting unit, and an adding / integrating unit which are connected in series.

Claim 3. (previously presented) Carrier recovery means according to claim 2, **characterized in** that said subtracting / differentiating unit is adapted to receive said robust phase error signal as an input signal and to generate and output a differential signal.

Claim 4. (previously presented) Carrier recovery means according to claim 3, **characterized in** that said first limiting unit is adapted to receive said differential signal as an input signal and to generate and output a limited signal not exceeding given first lower and/or upper limits.

Claim 5. (previously presented) Carrier recovery means according to claim 4, **characterized in** that said adding/integrating unit is adapted to receive said limited differential signal as an input signal and to generate and output a sum signal.

Claim 6. (previously presented) Carrier recovery means according to claim 5, **characterized in** that a second limiting unit is provided which is connected in series to said adding/integrating unit, and

said second limiting unit is adapted to receive said sum signal as an input signal and to generate and output a limited signal not exceeding given second lower and/or upper limits.

Claim 7. (previously presented) Carrier recovery means according to claim 1, **characterized in** that said first phase error detecting means is adapted to generate and output a valid robust phase error signal of the received digital input signal when an amplitude of the received digital input signal is above a first threshold, and

said second phase error detecting means is adapted to use only said valid robust phase error signal as an input signal only for generating said frequency sensitive phase error signal.

Claim 8. (previously presented) Carrier recovery means according to claim 1, **characterized in** that lock detector means is provided which is adapted to receive a phase error signal and to generate and output a locking signal therefrom when said phase error signal and/or an average value thereof is beyond a second threshold.

Claim 9. (previously presented) Carrier recovery means according to claim 8, **characterized in** that said locking detector means is adapted to use said robust phase error signal and said valid robust phase error signal supplied by said first phase error detecting means.

Claim 10. (canceled)

Claim 11. (previously presented) A method of carrier recovery for recovering a carrier of a received digital input signal in a channel decoding unit or a digital demodulating unit of a digital broadcasting receiver, comprising the steps of:

detecting a robust estimate of the phase error for the received digital input signal;

generating and outputting a robust phase error signal representative of said robust phase error; and

deriving a frequency sensitive phase error signal from the robust phase error signal, said frequency sensitive phase error signal being representative of the sign of the frequency error with respect to the received digital input signal and being used to reduce the frequency error with respect to the received digital signal to enable locking to at least the carrier thereof.

Claim 12. (previously presented) The method according to claim 11, wherein said frequency sensitive phase error signal is detected by a second phase error detector comprising at least a subtracting / differentiating unit, a first limiting unit, and an adding / integrating unit which are connected in series.

Claim 13. (previously presented) The method according to claim 12, wherein said subtracting / differentiating unit is adapted to receive said robust phase error signal as an input signal and to generate and output a differential signal.

Claim 14. (previously presented) The method according to claim 13, wherein said first limiting unit is adapted to receive said differential signal as an input signal and to generate and output a limited signal not exceeding given first lower and/or upper limits.

Claim 15. (previously presented) The method according to claim 14, wherein said adding/integrating unit is adapted to receive said limited differential signal as an input signal and to generate and output a sum signal.

Claim 16. (previously presented) The method according to claim 15, wherein a second limiting unit is provided which is connected in series to said adding/integrating unit, and is adapted to receive said sum signal as an input signal and to generate and output a limited signal not exceeding given second lower and/or upper limits.

Claim 17. (previously presented) The method according to claim 11, further comprising a step of generating and outputting a valid robust phase error signal of the received digital input signal when an amplitude of the received digital input signal is above a first threshold, and

generating said frequency sensitive phase error signal using only said valid robust phase error signal as an input signal.

Claim 18. (previously presented) The method according to claim 11, further comprising a step of generating and outputting a locking signal from a phase error signal when said phase error signal and/or an average value thereof is beyond a second threshold.

Claim 19. (previously presented) The method according to claim 18, wherein said locking signal is generated using said robust phase error signal and said valid robust phase error signal.